II. REMARKS

Claims 1-31 and 33-57 are pending, and claims 15-24 and 43-52 are allowed. The Applicant's attorney has amended claims 1, 3-7, 9, 11-14, 21-24, 26-30, 33-37, 39-40, and 42, and has cancelled claim 32 without prejudice or disclaimer. But the amendments to claims 3, 12, 21-24, 26-29, and 40 do not narrow these claims. In light of the following, all of the claims as amended are now in condition for allowance, and, therefore, the Applicant's attorney requests the Examiner to withdraw all of the outstanding rejections.

Amendments to the Specification

The Applicant's attorney has amended the specification to correct typographical and grammatical errors, but these amendments add no new matter to the patent application.

Rejection of Claims 1-4, 8-14, 25-33, 37-42, and 53-57 Under 35 U.S.C. § 102(b) As Being Anticipated By "VLSI Implementation Of Inverse Discrete Cosine Transformer . . .", Masaki et al.

As discussed below, the Applicants' attorney disagrees with this rejection.

Claim 1

Claim 1 as amended recites a processor operable to store in a row of a memory intermediate values from first and second matrix columns, to combine the stored intermediate values within the row to generate resulting values for third and fourth matrix columns, and to store the resulting values in respective rows of the memory.

For example, referring, *e.g.*, to p. 12 and FIGS. 12-18 of the patent application, a computing unit 112 (FIG. 13) of a processor 108 (FIG. 12) stores in a row Reg0 Masaki values de_{00} and do_{00} (intermediate values) from the left most matrix columns (top and bottom) of equation (12). Per equation (13), the unit 112 computes ½ the sum and ½ the difference of de_{00} and do_{00} (combines de_{00} and do_{00}) to generate resulting values I'_{00} and I'_{07}, which are intermediate inverse-transform values, for the leftmost matrix columns of equation (13). Referring to FIGS. 17 and 18, the computing unit 112 then respectively

stores I'_{00} and I'_{07} in rows Reg1 and Reg2, and thus effectively transposes the I' matrix without executing a separate transpose instruction.

Conversely, Masaki does not disclose combining intermediate values that are stored within the same row of memory, nor does Masaki disclose storing resulting values in respective rows of memory. Referring, *e.g.*, to equations (6) and (7) and FIGS. 5 and 6(a), Masaki stores (intermediate) values $x_{o0} - x_{o3}$ and $x_{e0} - x_{e3}$ — x_o and x_e respectively represent the same quantities as do and de above — in different shift registers (rows), and thus does not combine values that are in the same register. For example, as shown in FIG. 5, Masaki combines x_{o0} and x_{e0} from different shift registers to generate (resulting) values x_0 and x_7 — x represents the same quantity as I' above. Furthermore, Masaki stores the (resulting) values x_0 - x_7 in the same row (the top row of FIG. 6(a) in the positions marked "1"), not in different rows.

Claims 2-3 and 8

These claims are patentable by virtue of their dependencies on claim 1.

Claim 9

Claim 9 as amended recites a processor operable to combine a first matrix column of first intermediate values with a second matrix column of second intermediate values to generate a set of resulting values and to store the set of resulting values in more than one memory row.

For example, referring, *e.g.*, to p. 12 and FIGS. 12-18 of the patent application, a computing unit 112 (FIG. 13) of a processor 108 (FIG. 12) computes ½ the sum of and ½ the difference between even Masaki values de_{00} - de_{03} from a first matrix column and respective odd Masaki values do_{00} - do_{03} from a second matrix column to generate a set of resulting values I'_{00} - I'_{07}. Referring to FIGS. 17 and 18, the computing unit 112 then stores I'_{00} - I'_{07} in respective rows (Reg1 . . .) to effectively transpose the I' matrix without executing a separate transpose instruction.

Conversely, Masaki does not disclose storing a set of resulting values in more than one memory row. Referring, *e.g.,* to FIG. 6(a), Masaki stores a set of resulting values x_0 - x_7 in a single row (the top row of FIG. 6(a)), not in respective rows.

Claims 10-13

These claims are patentable by virtue of their dependencies from claim 9.

Claim 25

Claim 25 recites a processor operable to store pixel values that respectively occupy every other position of a row in a first continuous section of a register and to store the pixel values that respectively occupy remaining positions of the row in a second continuous section of the register.

For example, referring to FIGS. 3, 13 and 16 and equation (12) (p. 12) of the patent application, a computing unit 112 (FIG. 13) of a processor 108 (FIG. 12) receives discrete cosine transform (pixel) values $D_{00} - D_{07}$ (FIG. 3) that each occupy a respective position within a row of pixel values. Because equation (12) requires that these values be rearranged into even and odd matrix columns D_{00}, D_{02}, D_{04}, D_{06} and D_{01}, D_{03}, D_{05}, D_{07}, the unit 112 executes an inverse zig-zag operation that stores in the left half (a first continuous section) of a register 136a (FIG. 16) the pixel values (*e.g,* D_{00}, D_{02}, D_{04}, D_{06}) that occupy every other position of the row, and stores in the right half (second continuous section) of the register 136a the pixel values (*e.g.,* D_{01}, D_{03}, D_{05}, D_{07}) that occupy the remaining positions of the row.

In contrast, Masaki does not disclose storing pixel values that respectively occupy every other position of a row in a first continuous section of a register, or storing the pixel values that respectively occupy remaining positions of the row in a second continuous section of the register. Referring, *e.g.,* to FIG. 5, Masaki generates first and second groups $x_3 - x_0$ and $x_4 - x_7$ of intermediate inverse-transform values, and inverts the order of the first group ($x_3 - x_0 \rightarrow x_0 - x_3$) such that the top row of the memory (FIG. 6(a)) contains x_0 - x_7 in the positions 1, 2, 3, 4, 4, 3, 2, 1 respectively. But inverting the order of first group x_3

– x_0 is not the same as the claimed technique, which would yield x_3, x_1, x_4, x_6, x_2, x_0, x_5, x_7 in the top row of Masaki's memory.

Claims 26-29

These claims are patentable by virtue of their dependencies from claim 25.

Claim 30

Claim 30 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 1.

Claims 31-33

These claims are patentable by virtue of their dependencies from claim 30.

Claim 37

Claim 37 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 9.

Claims 38-42

These claims are patentable by virtue of their dependencies from claim 37.

Claim 53

Claim 53 is patentable for reasons similar to those discussed above in support of the patentability of claim 25.

Claim 54 - 57

These claims are patentable by virtue of their dependencies on claim 53.

Objection To Claims 5-7 and 34-36

The Applicant's attorney has rewritten these claims in allowable form.

Conclusion

In light of the foregoing, claims 2, 8, 10, 15-20, 25, 31, 38, 41, and 43-57 as previously pending and claims 1, 3-7, 9, 11-14, 21-24, 26-30, 33-37, 39-40, and 42 as amended are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicant's attorney, Bryan Santarelli, at (425) 455-5575.

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Respectfully Submitted,

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